

## QUAD LOW-SIDE DRIVER IC

 Check for Samples: [DRV8803](#)

### FEATURES

- **4-Channel Protected Low-Side Driver**
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Catch Diodes
  - Parallel Interface
- **1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)**

- **8.2-V to 60-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

### APPLICATIONS

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

### DESCRIPTION

The DRV8803 provides a 4-channel low side driver with overcurrent protection. It has built-in diodes to clamp turn-off transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

The DRV8803 can supply up to 1.5-A (single channel on) or 800-mA (four channels on) continuous output current (with adequate PCB heatsinking at 25°C).

The device is controlled via a simple parallel interface.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8803 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	(SOIC) - DW	Reel of 2000	DRV8803DWR	DRV8803
		Tube of 25	DRV8803DW	DRV8803
	(HTSSOP) - PWP	Consult Factory		

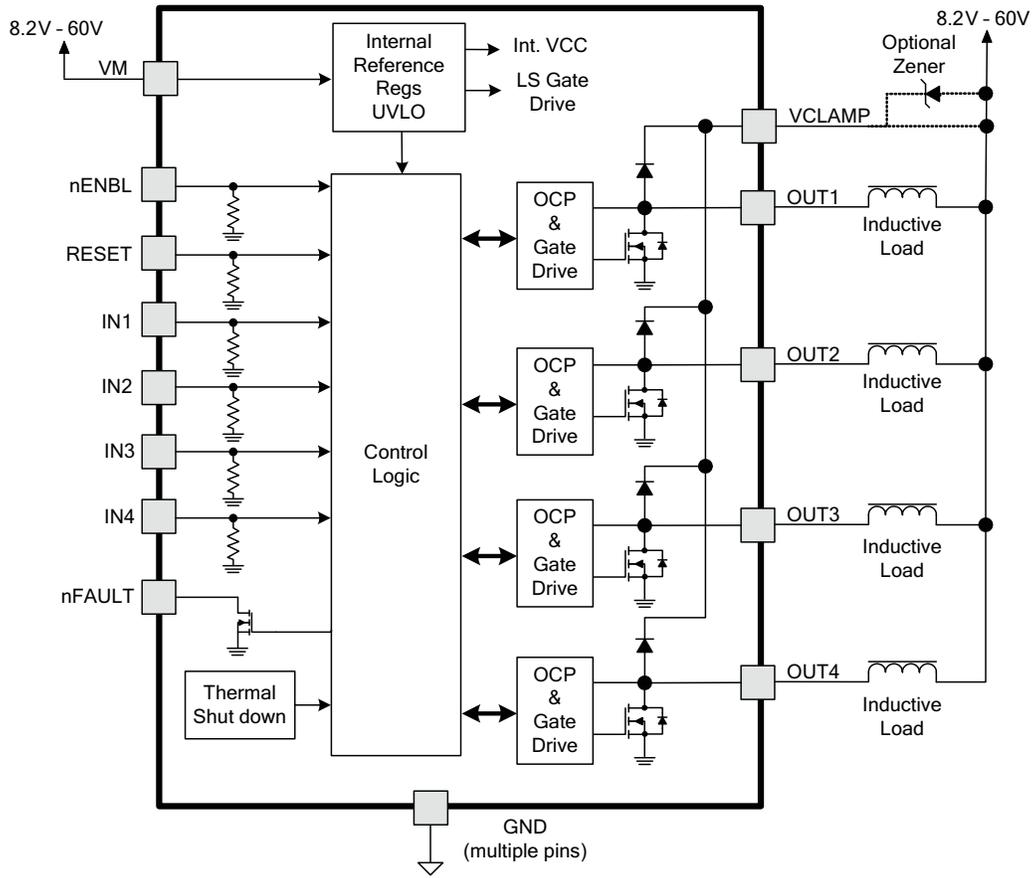
(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



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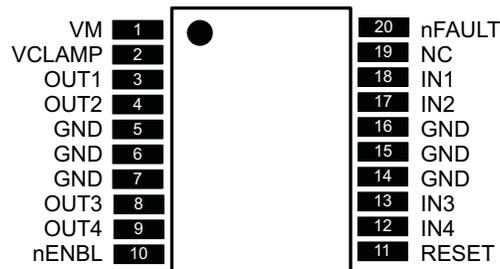
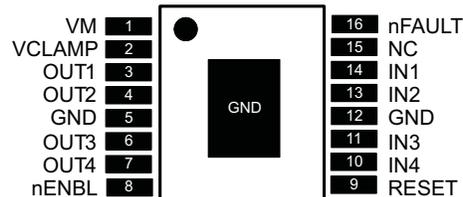
**DEVICE INFORMATION**  
**Functional Block Diagram**



**Table 1. TERMINAL FUNCTIONS**

NAME	PIN (SOIC)	PIN (HTSSOP)	I/O <sup>(1)</sup>	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
<b>POWER AND GROUND</b>					
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	-	Device ground	All pins must be connected to GND.
VM	1	1	-	Device power supply	Connect to motor supply (8.2 V - 60 V).
<b>CONTROL</b>					
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active high resets internal logic and OCP – internal pulldown
IN1	18	14	I	Channel 1 input	IN1 = 1 drives OUT1 low – internal pulldown
IN2	17	13	I	Channel 2 input	IN2 = 1 drives OUT2 low – internal pulldown
IN3	13	11	I	Channel 3 input	IN3 = 1 drives OUT3 low – internal pulldown
IN4	12	10	I	Channel 4 input	IN4 = 1 drives OUT4 low – internal pulldown
<b>STATUS</b>					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
<b>OUTPUT</b>					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	-	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

**DW (WIDE SOIC) PACKAGE  
(TOP VIEW)**

**PWP (HTSSOP) PACKAGE  
(TOP VIEW)**


## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		VALUE	UNIT
V <sub>M</sub>	Power supply voltage range	–0.3 to 65	V
V <sub>OUTx</sub>	Output voltage range	–0.3 to 65	V
V <sub>CLAMP</sub>	Clamp voltage range	–0.3 to 65	V
nFAULT	Output current	20	mA
	Peak clamp diode current	1.5	A
	DC or RMS clamp diode current	1	A
	Digital input pin voltage range	–0.5 to 7	V
nFAULT	Digital output pin voltage range	–0.5 to 7	V
	Peak motor drive output current, t < 1 μS	Internally limited	A
	Continuous total power dissipation	See Dissipation Ratings table	
T <sub>J</sub>	Operating virtual junction temperature range	–40 to 150	°C
T <sub>stg</sub>	Storage temperature range	–60 to 150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## THERMAL INFORMATION

THERMAL METRIC		DRV8803	UNITS
		DW	
		20 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	67.7	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance <sup>(2)</sup>	32.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(3)</sup>	35.4	
ψ <sub>JT</sub>	Junction-to-top characterization parameter <sup>(4)</sup>	8.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter <sup>(5)</sup>	34.9	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance <sup>(6)</sup>	N/A	

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
$V_M$	Power supply voltage range	8.2		60	V
$V_{CLAMP}$	Output clamp voltage range	8.2		60	V
$I_{OUT}$	Continuous output current, single channel on, $T_A = 25^\circ\text{C}$ , SOIC package <sup>(1)</sup>			1.5	A
	Continuous output current, four channels on, $T_A = 25^\circ\text{C}$ , SOIC package <sup>(1)</sup>			0.8	
	Continuous output current, single channel on, $T_A = 25^\circ\text{C}$ , HTSSOP package <sup>(1)</sup>			1.5	
	Continuous output current, four channels on, $T_A = 25^\circ\text{C}$ , HTSSOP package <sup>(1)</sup>			0.8	

(1) Power dissipation and thermal limits must be observed.

**ELECTRICAL CHARACTERISTICS**

$T_A = 25^\circ\text{C}$ , over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES</b>						
$I_{VM}$	VM operating supply current	$V_M = 24\text{ V}$		1.6	2.1	mA
$V_{UVLO}$	VM undervoltage lockout voltage	$V_M$ rising			8.2	V
<b>LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)</b>						
$V_{IL}$	Input low voltage			0.6	0.7	V
$V_{IH}$	Input high voltage		2			V
$V_{HYS}$	Input hysteresis			0.45		V
$I_{IL}$	Input low current	$V_{IN} = 0$	-20		20	$\mu\text{A}$
$I_{IH}$	Input high current	$V_{IN} = 3.3\text{ V}$			100	$\mu\text{A}$
$R_{PD}$	Pulldown resistance			100		k $\Omega$
<b>nFAULT OUTPUT (OPEN-DRAIN OUTPUT)</b>						
$V_{OL}$	Output low voltage	$I_O = 5\text{ mA}$			0.5	V
$I_{OH}$	Output high leakage current	$V_O = 3.3\text{ V}$			1	$\mu\text{A}$
<b>LOW-SIDE FETS</b>						
$R_{DS(ON)}$	FET on resistance	$V_M = 24\text{ V}$ , $I_O = 700\text{ mA}$ , $T_J = 25^\circ\text{C}$		0.5		$\Omega$
		$V_M = 24\text{ V}$ , $I_O = 700\text{ mA}$ , $T_J = 85^\circ\text{C}$		0.75	0.8	
$I_{OFF}$	Off-state leakage current		-50		50	$\mu\text{A}$
<b>HIGH-SIDE DIODES</b>						
$V_F$	Diode forward voltage	$V_M = 24\text{ V}$ , $I_O = 700\text{ mA}$ , $T_J = 25^\circ\text{C}$		1.2		V
$I_{OFF}$	Off-state leakage current	$V_M = 24\text{ V}$ , $T_J = 25^\circ\text{C}$	-50		50	$\mu\text{A}$
<b>OUTPUTS</b>						
$t_R$	Rise time	$V_M = 24\text{ V}$ , $I_O = 700\text{ mA}$ , Resistive load	50		300	ns
$t_F$	Fall time	$V_M = 24\text{ V}$ , $I_O = 700\text{ mA}$ , Resistive load	50		300	ns
<b>PROTECTION CIRCUITS</b>						
$I_{OCP}$	Overcurrent protection trip level		2.3		3.8	A
$t_{OCP}$	Overcurrent protection deglitch time			3.5		$\mu\text{s}$
$t_{RETRY}$	Overcurrent protection retry time			1.2		ms
$t_{TSD}$	Thermal shutdown temperature	Die temperature <sup>(1)</sup>	150	160	180	$^\circ\text{C}$

(1) Not production tested.

### TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		50	ns
2	$t_{PD(L-H)}$	Propogation delay time, INx to OUTx, low to high		200	ns
3	$t_{PD(H-L)}$	Propogation delay time, INx to OUTx, high to low		200	ns
-	$t_{RESET}$	RESET pulse width	20		$\mu$ s

(1) Not production tested.

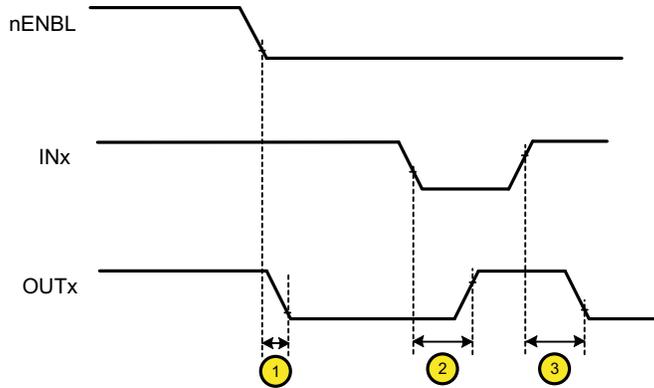


Figure 1. DRV8803 Timing Requirements

## FUNCTIONAL DESCRIPTION

### Output Drivers

The DRV8803 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

### Parallel Interface Operation

The DRV8803 is controlled with a simple parallel interface. Logically, the interface is shown in [Figure 2](#).

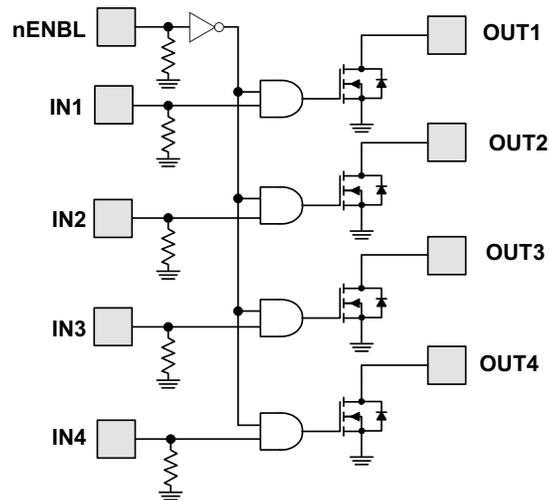


Figure 2. Parallel Interface Operation

### nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic. All inputs are ignored while RESET is active. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power-up.

## Protection Circuits

The DRV8803 is fully protected against undervoltage, overcurrent and overtemperature events.

### Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the  $t_{OCP}$  deglitch time (approximately 3.5  $\mu$ s), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the  $t_{RETRY}$  retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

### Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

## THERMAL INFORMATION

### Thermal Protection

The DRV8803 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### Power Dissipation

Power dissipation in the DRV8803 is dominated by the power dissipated in the output FET resistance, or  $R_{DS(ON)}$ . Average power dissipation of each FET when running a static load can be roughly estimated by [Equation 1](#):

$$P = R_{DS(ON)} \cdot (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one FET,  $R_{DS(ON)}$  is the resistance of each FET, and  $I_{OUT}$  is equal to the average current drawn by the load. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that  $R_{DS(ON)}$  increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### Heatsinking

The DRV8803 package uses a standard SOIC outline, but has the center pins internally fused to the die pad in order to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DRV8803DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV8803DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV8803PWP	PREVIEW	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DRV8803PWPR	PREVIEW	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

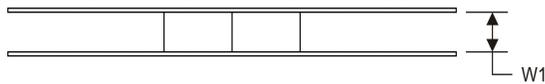
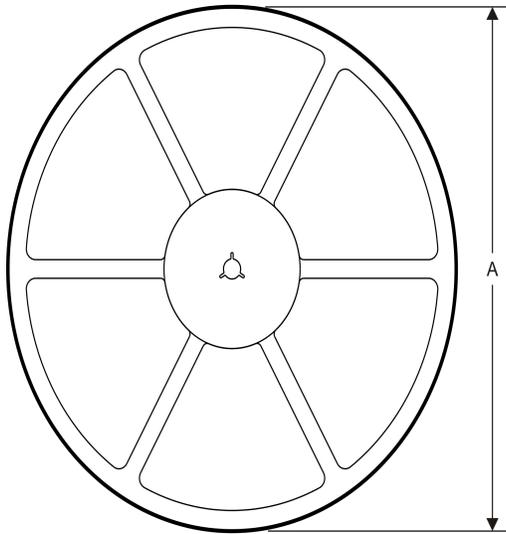
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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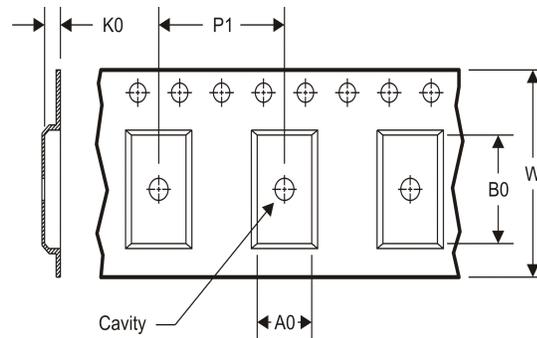
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



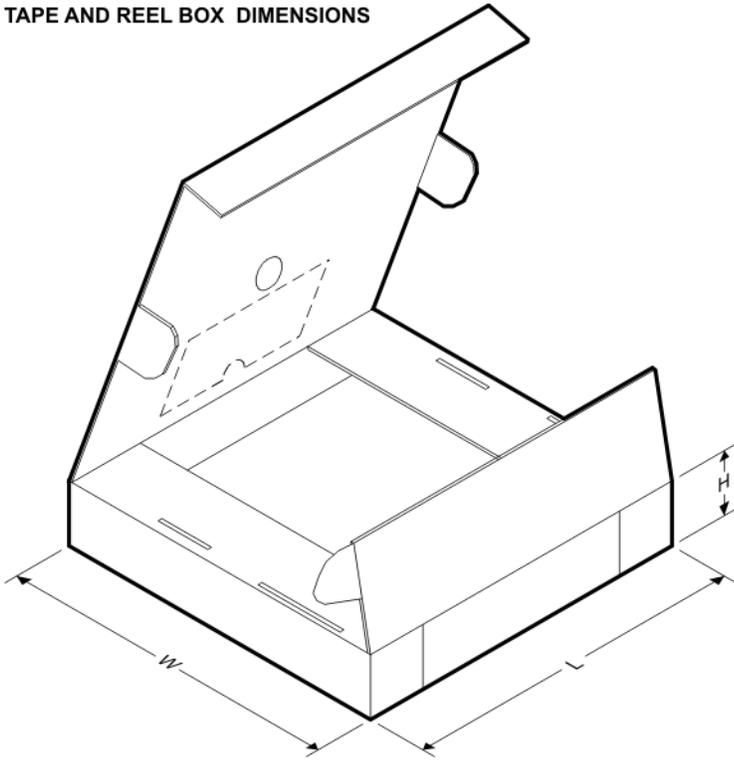
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8803DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

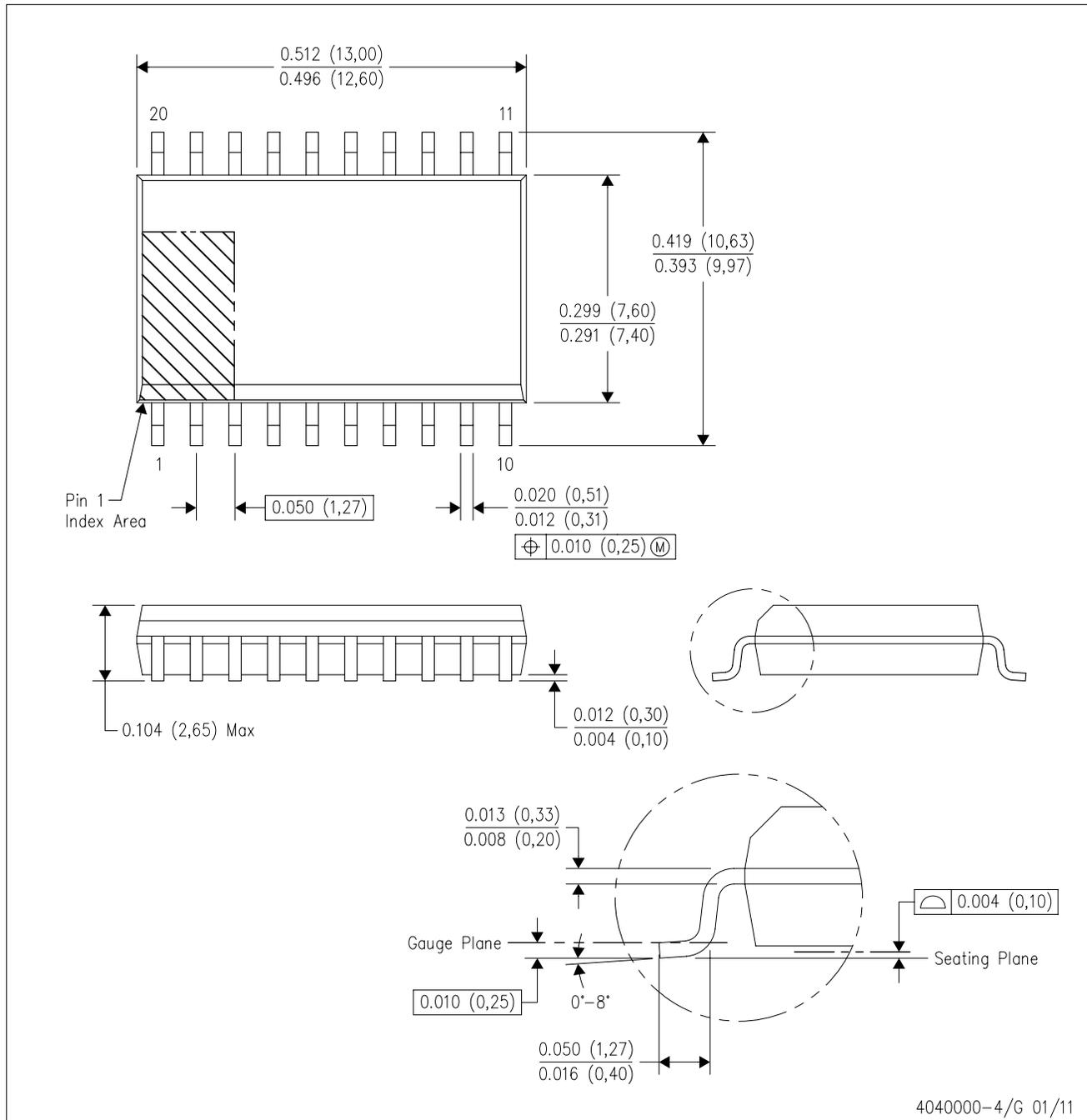


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8803DWR	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20)

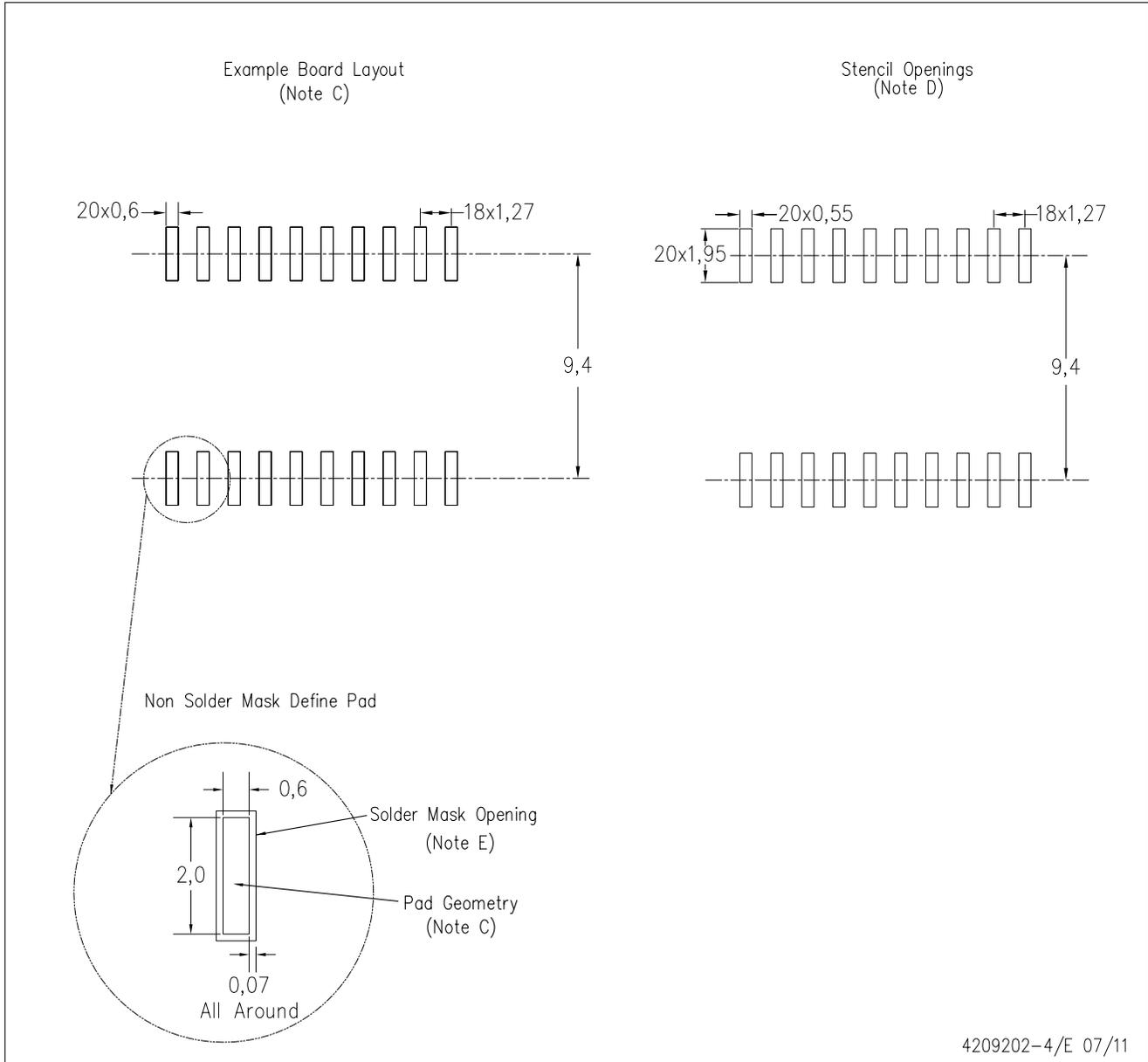
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

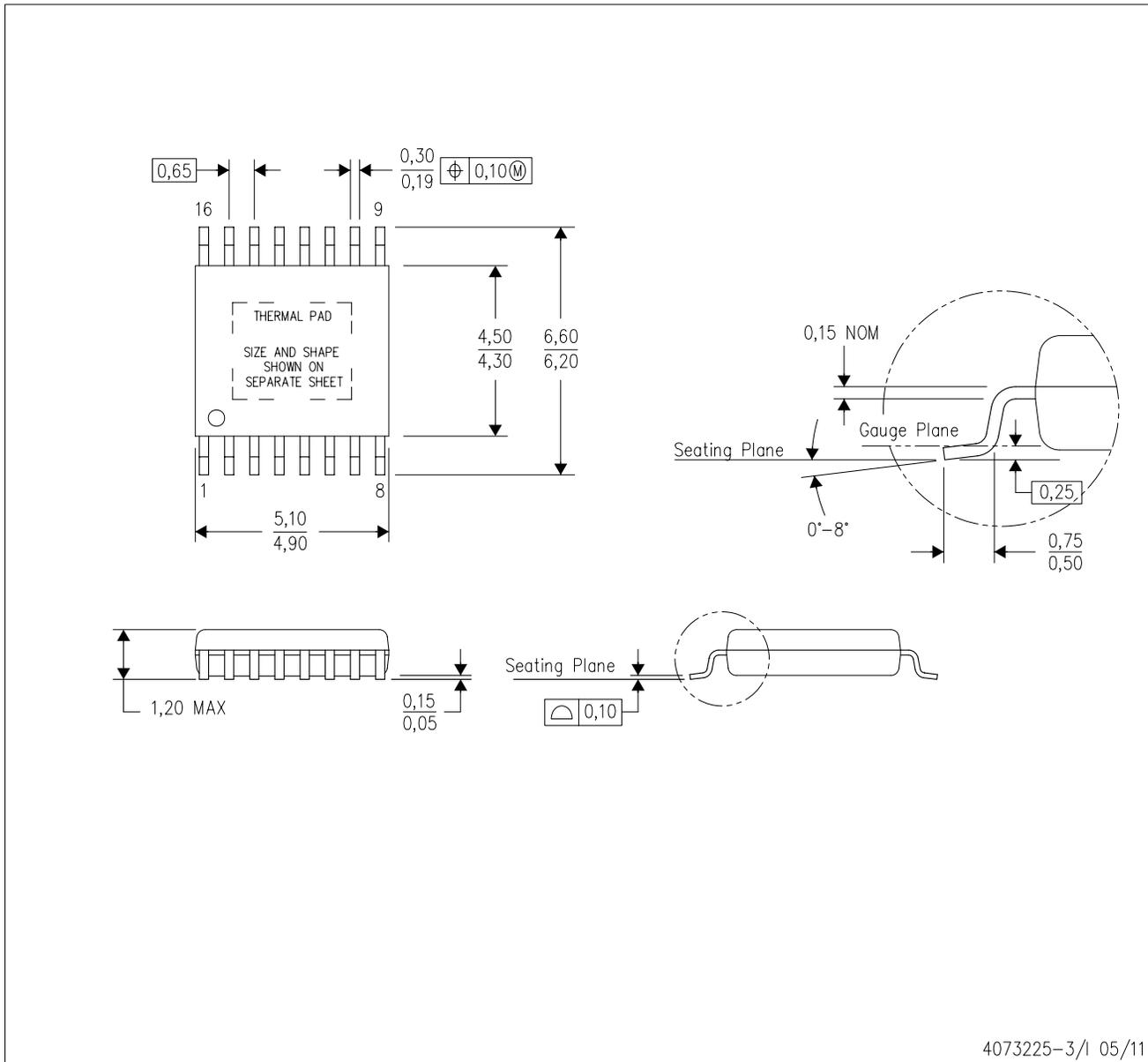


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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-3/1 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G16)

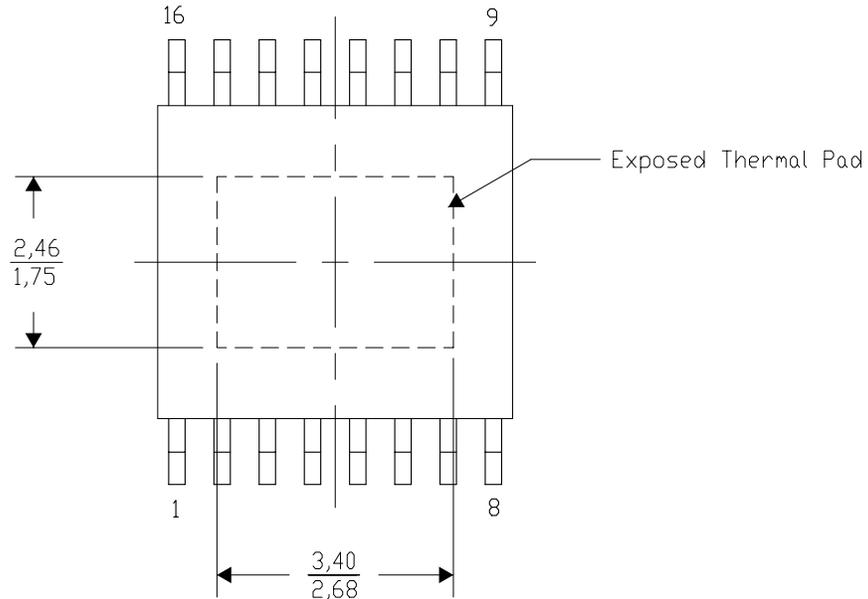
PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



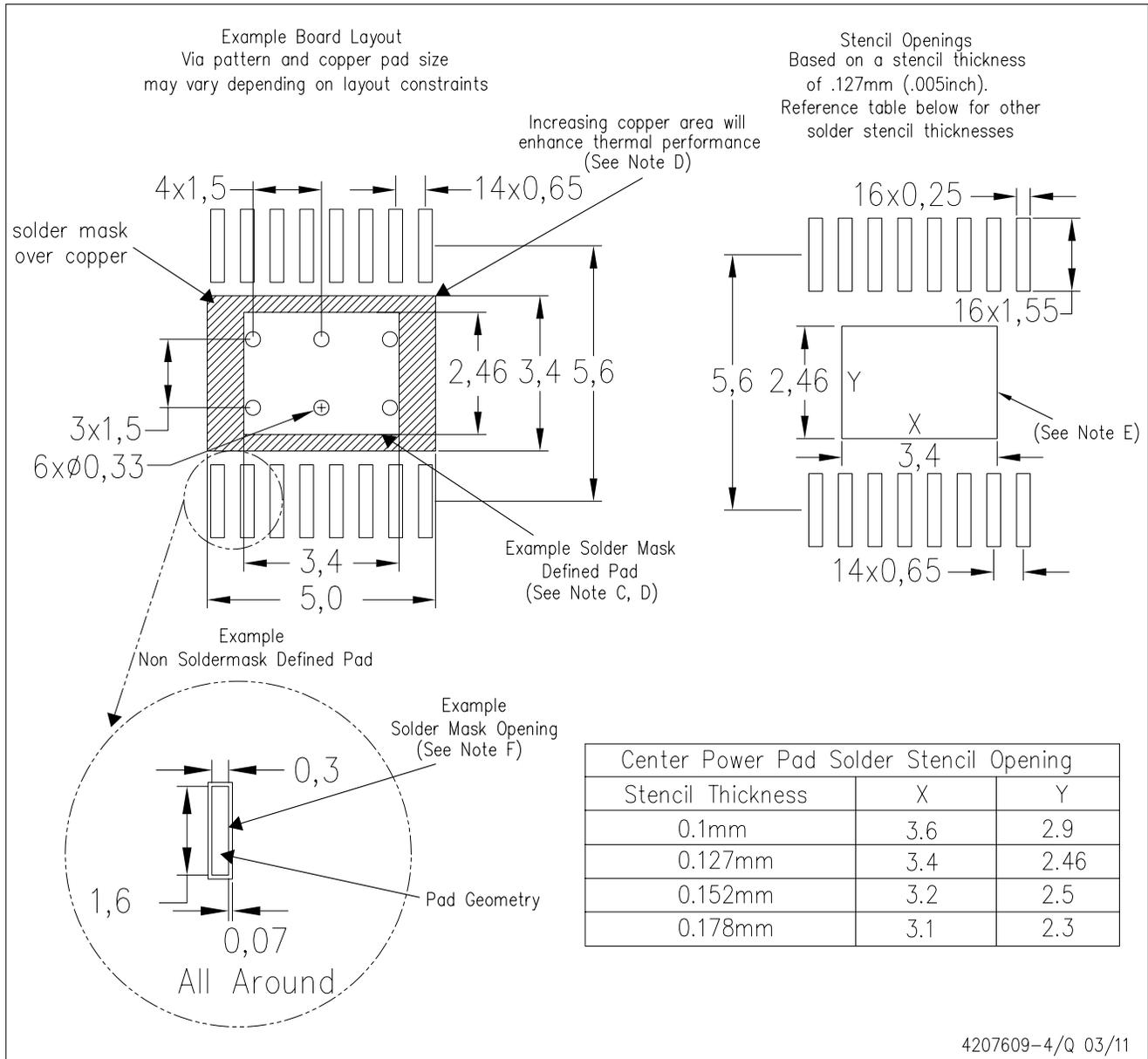
Top View

Exposed Thermal Pad Dimensions

4206332-7/Y 10/11

NOTE: A. All linear dimensions are in millimeters

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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